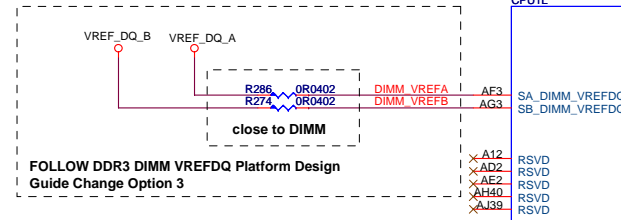
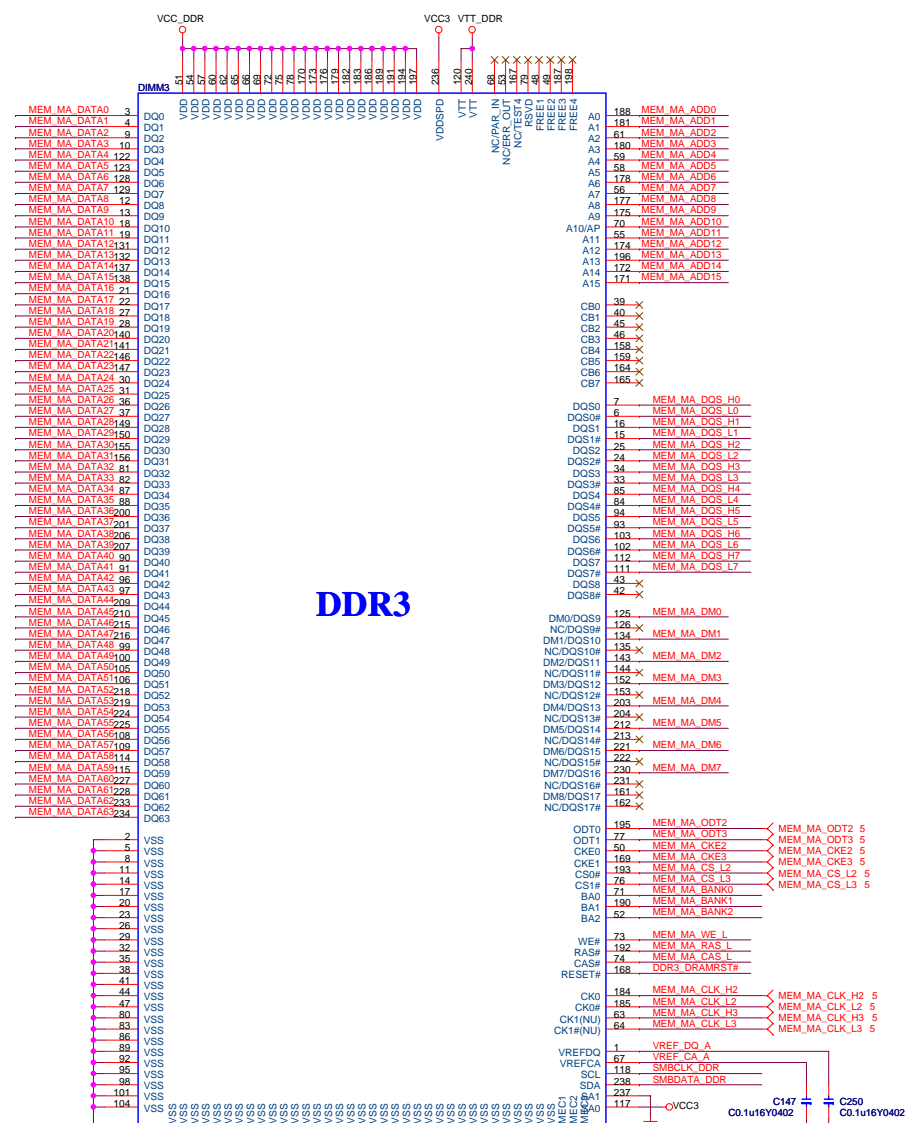


NOTE:R286,R274 STUFFED,JF DDR3 DIMM VREFDQ OPTION 2 UNSTUFFED.



DDRIII DIMM_A2



DDR3

UPI VOLTAGE CONSOLE

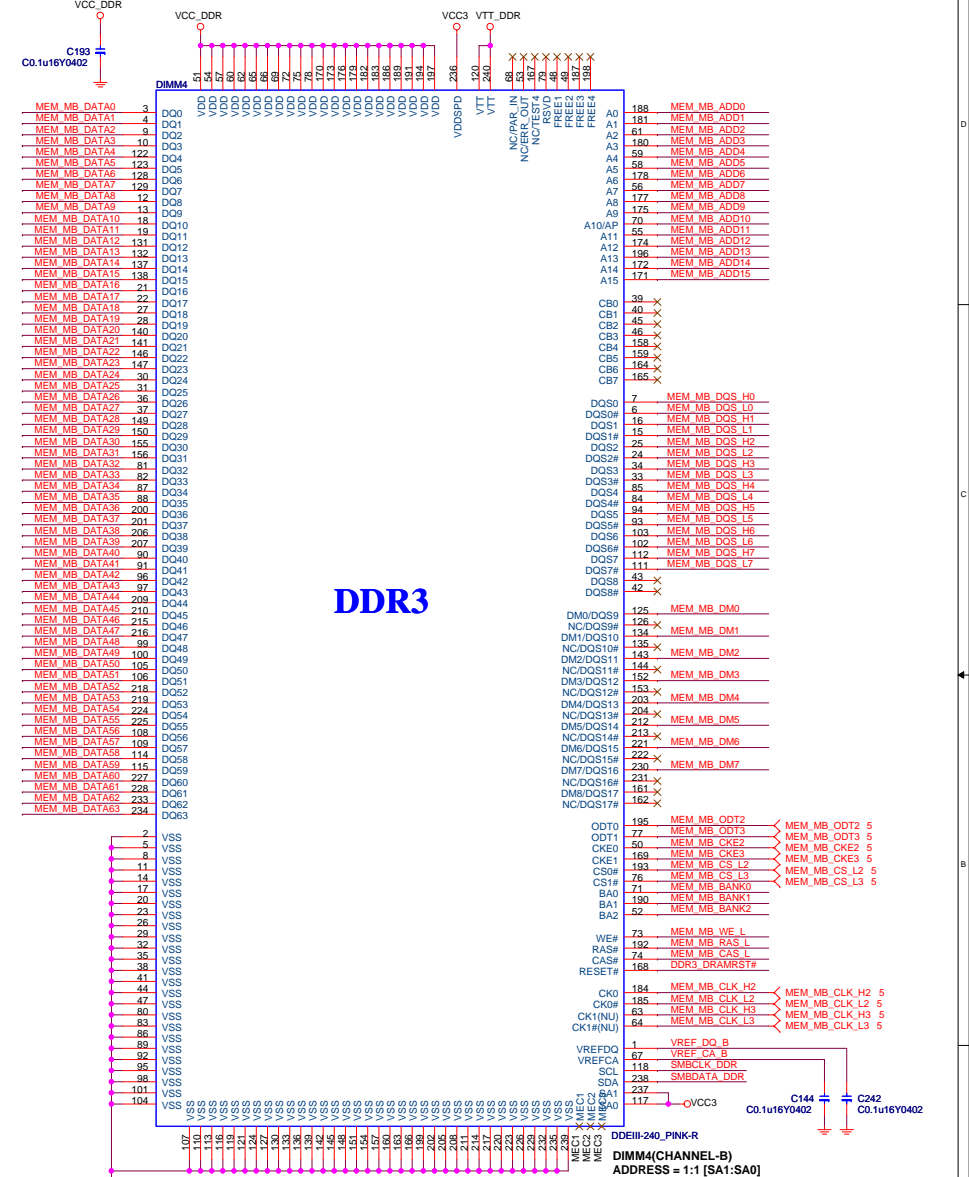
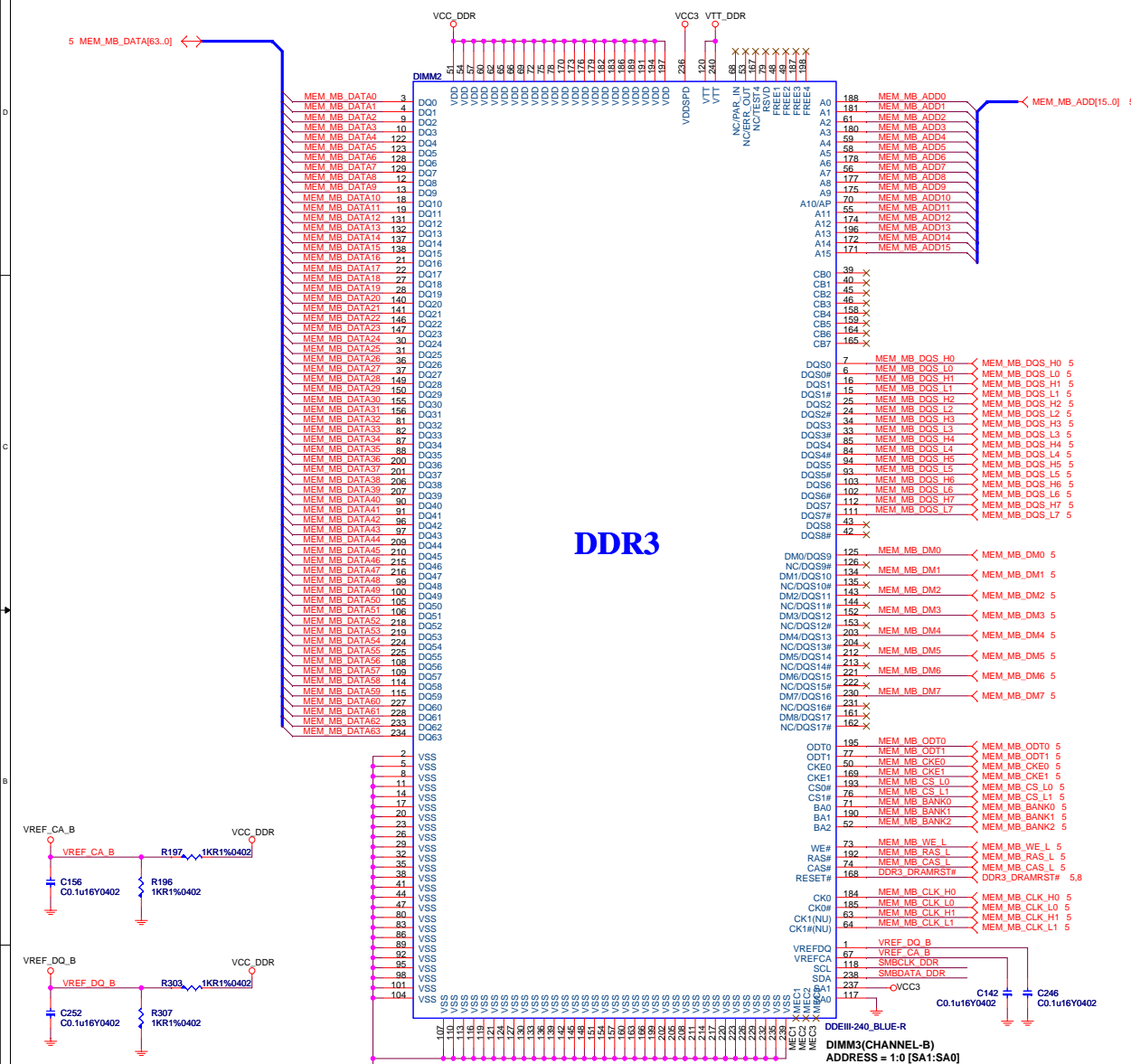
2.083325V

DIMM1(CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]

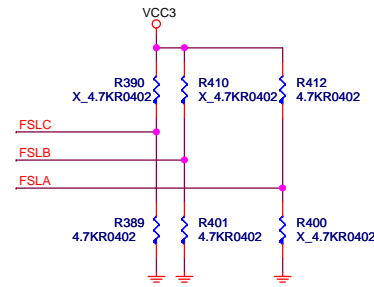
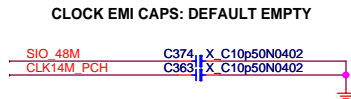
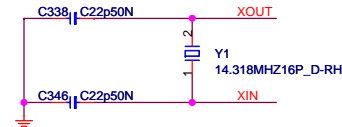
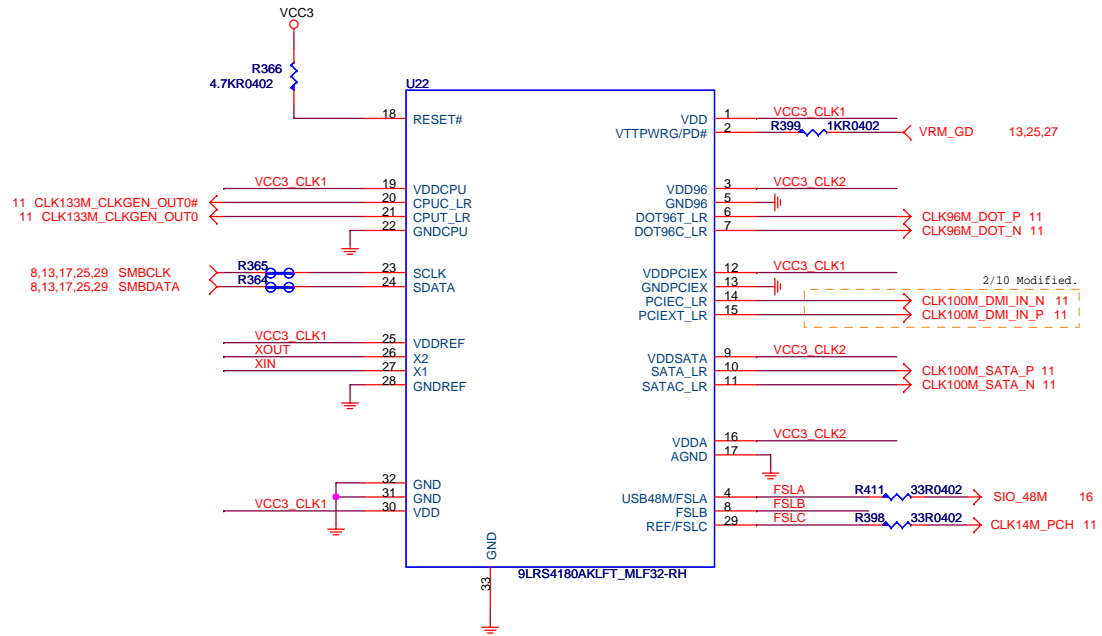
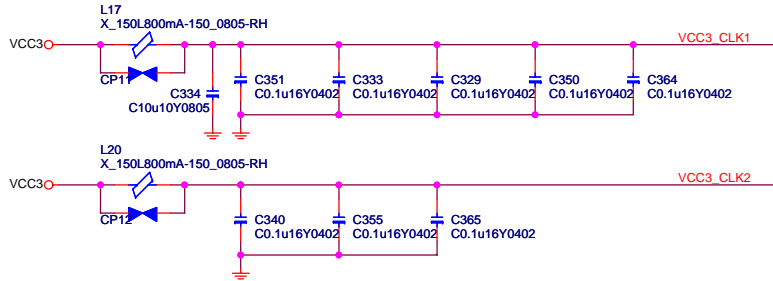
Title				DDR3 Chanel-A DIMM1/2			
Size	Document Number					Rev	
	DELL ShenYang Ecco H57					1.0	
Date:	Monday, November 02, 2009			Sheet	8	of	34

DDR3 DIMM_B1

DDR3 DIMM_B2



SMBCLK_DDR < SMBCLK_DDR 8
SMBDATA_DDR < SMBDATA_DDR 8



IBEXPEAK_A

PCI-E

USB

DMI

1 OF 9

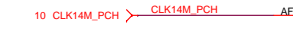
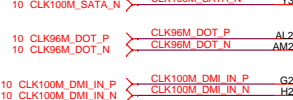
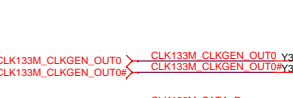
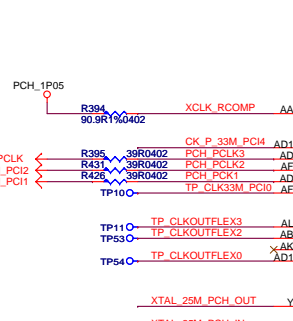
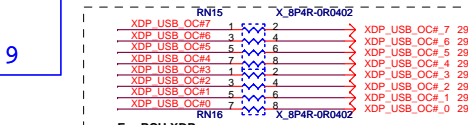
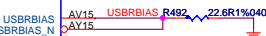
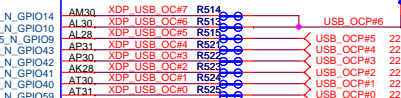
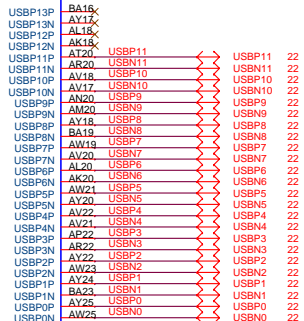
IBEX_0

IBEXPEAK_A

PCI

2 OF 9

IBEX_0



BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

WEAK INTERNAL PULLUPS ON GNT#

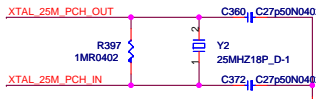
PGNT#1 R445 X 1KR0402
PGNT#0 R438 X 1KR0402

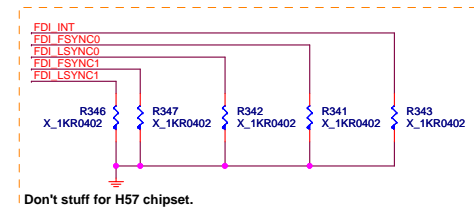
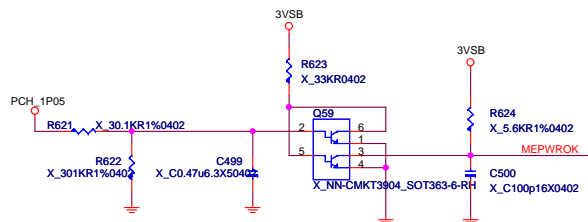


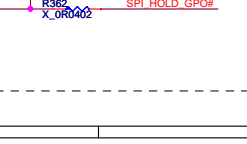
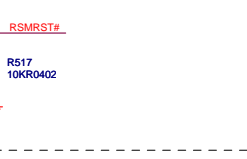
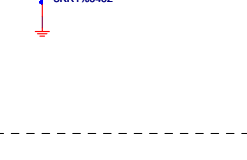
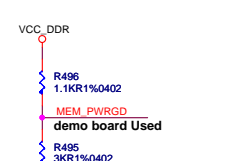
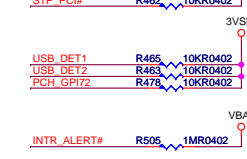
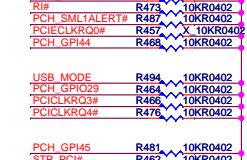
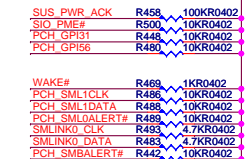
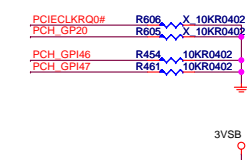
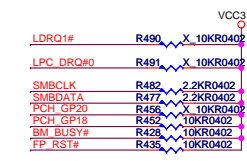
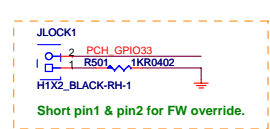
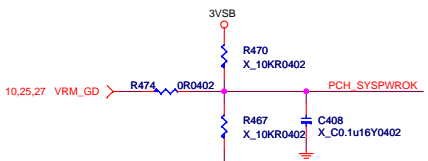
IBEXPEAK_A

CLOCK

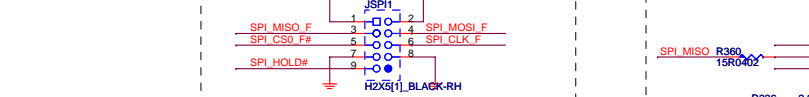
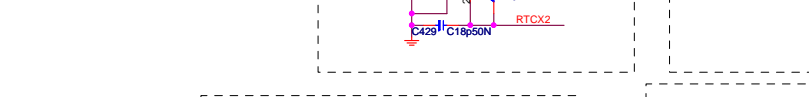
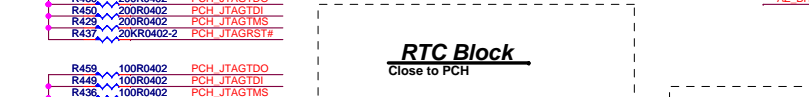
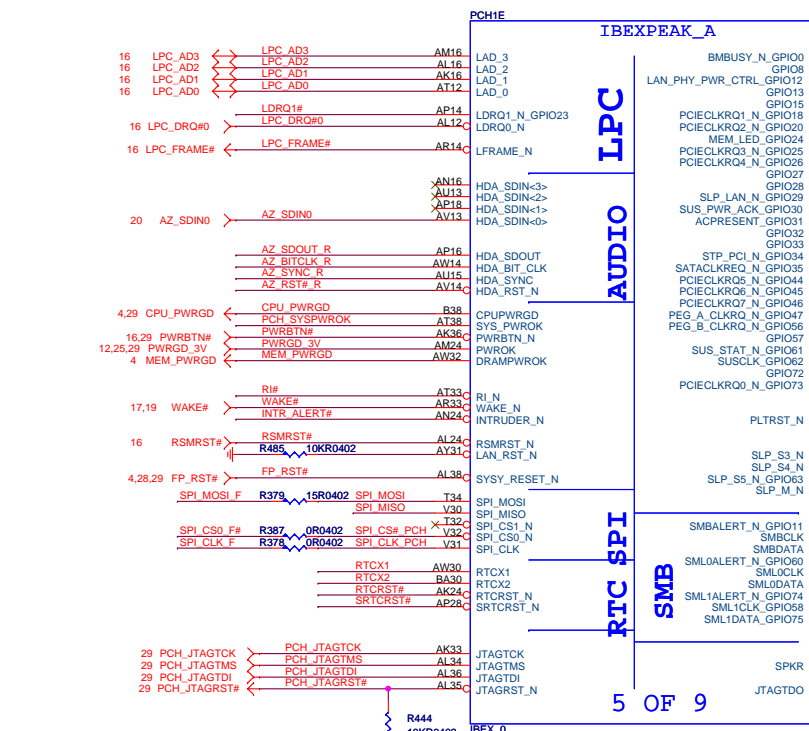
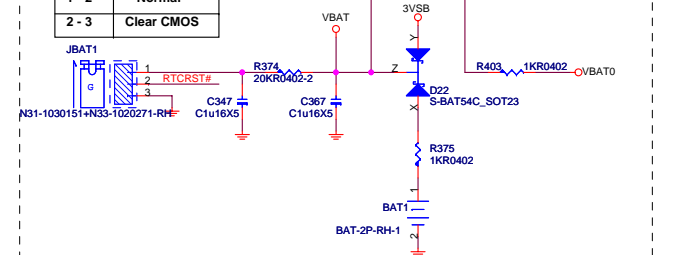
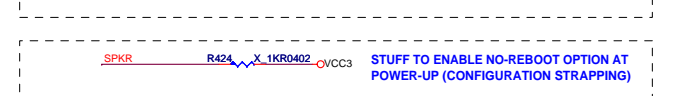
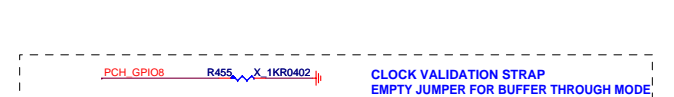
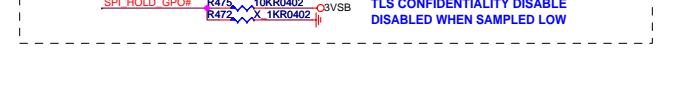
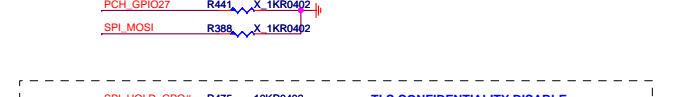
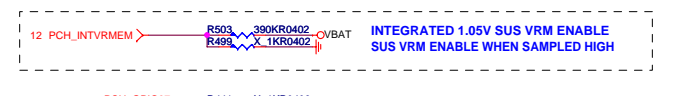
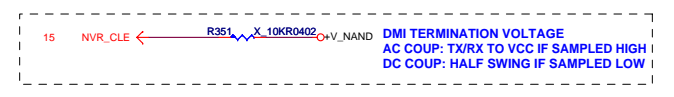
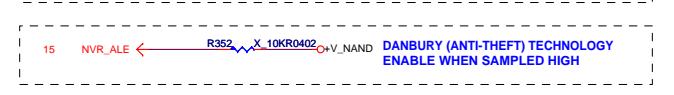
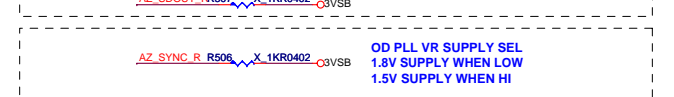
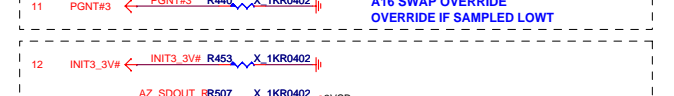
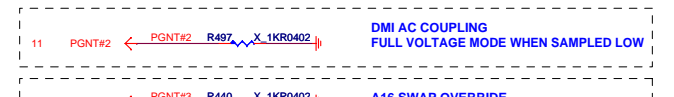
3 OF 9





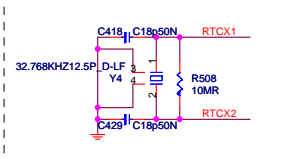


REQUIRED STRAPS



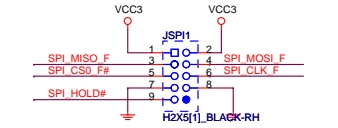
RTC Block

Close to PCH



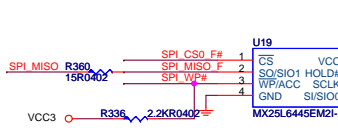
SPI DEBUG PROT

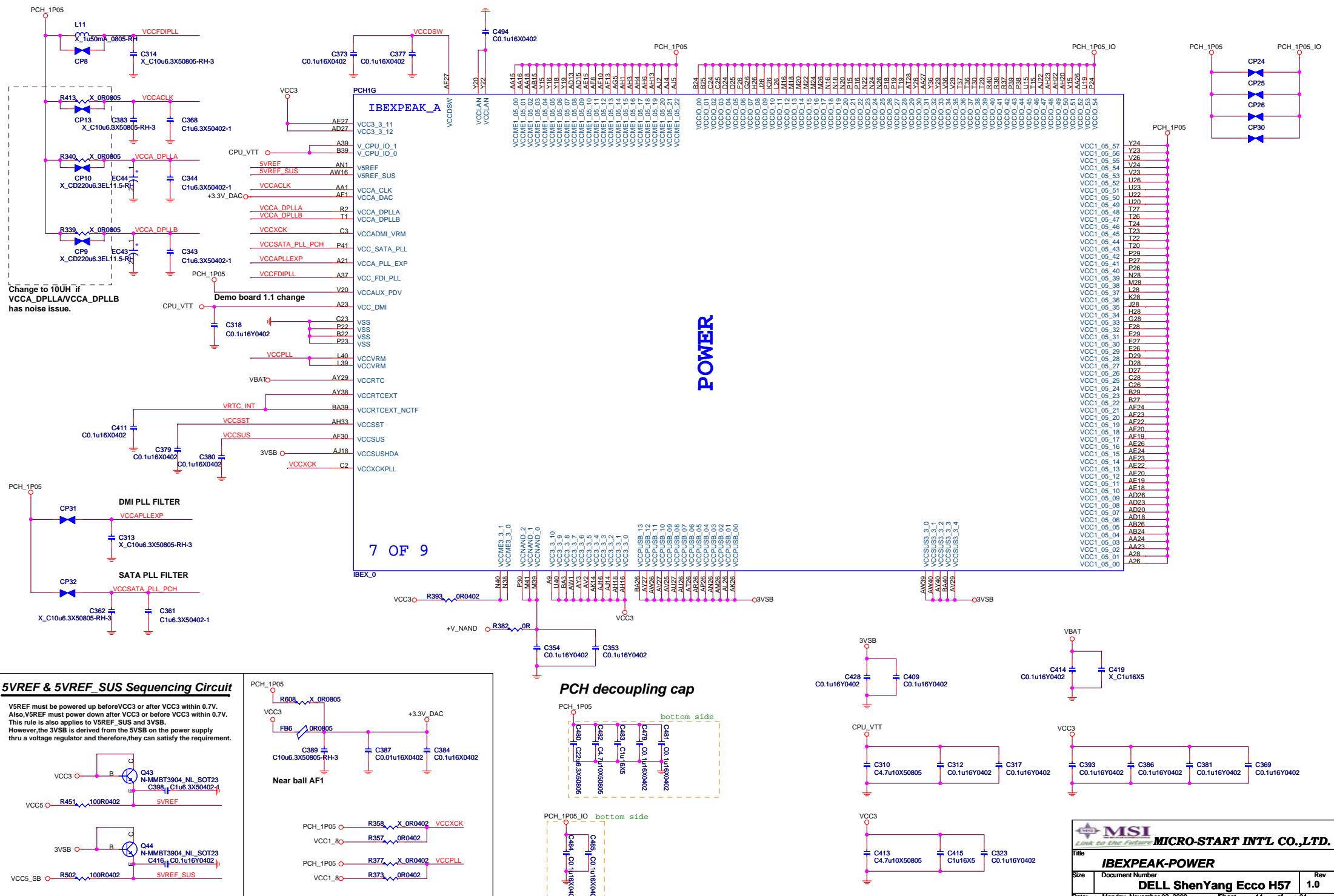
Close to SPI ROM



SPI FLASH ROM

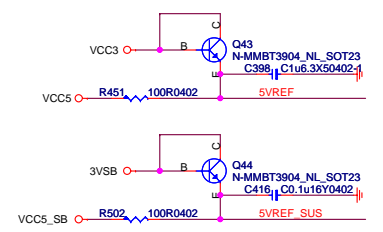
Place close to SB.



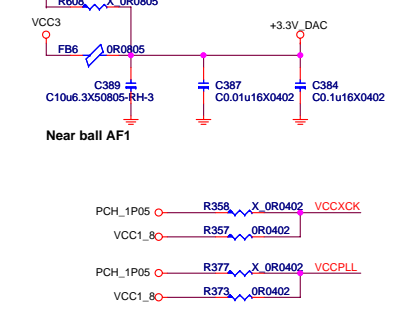


5VREF & 5VREF_SUS Sequencing Circuit

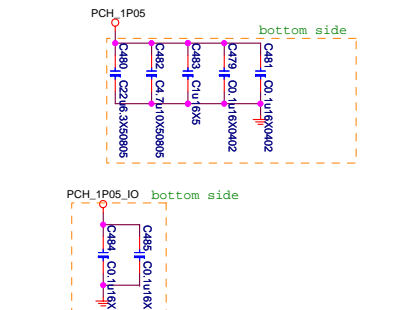
5VREF must be powered up before VCC3 or after VCC3 within 0.7V. Also, 5VREF must power down after VCC3 or before VCC3 within 0.7V. This rule is also applies to 5VREF_SUS and 3VSB. However, the 3VSB is derived from the 5VSB on the power supply thru a voltage regulator and therefore, they can satisfy the requirement.



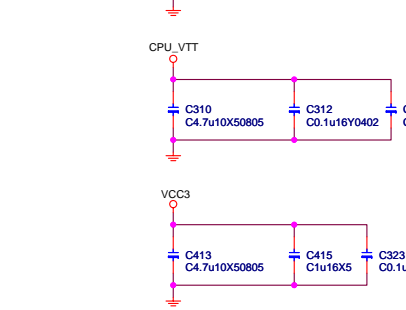
PCH decoupling cap



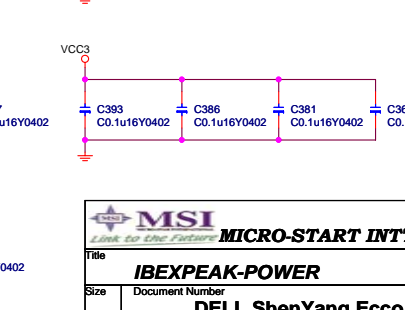
SATA PLL FILTER

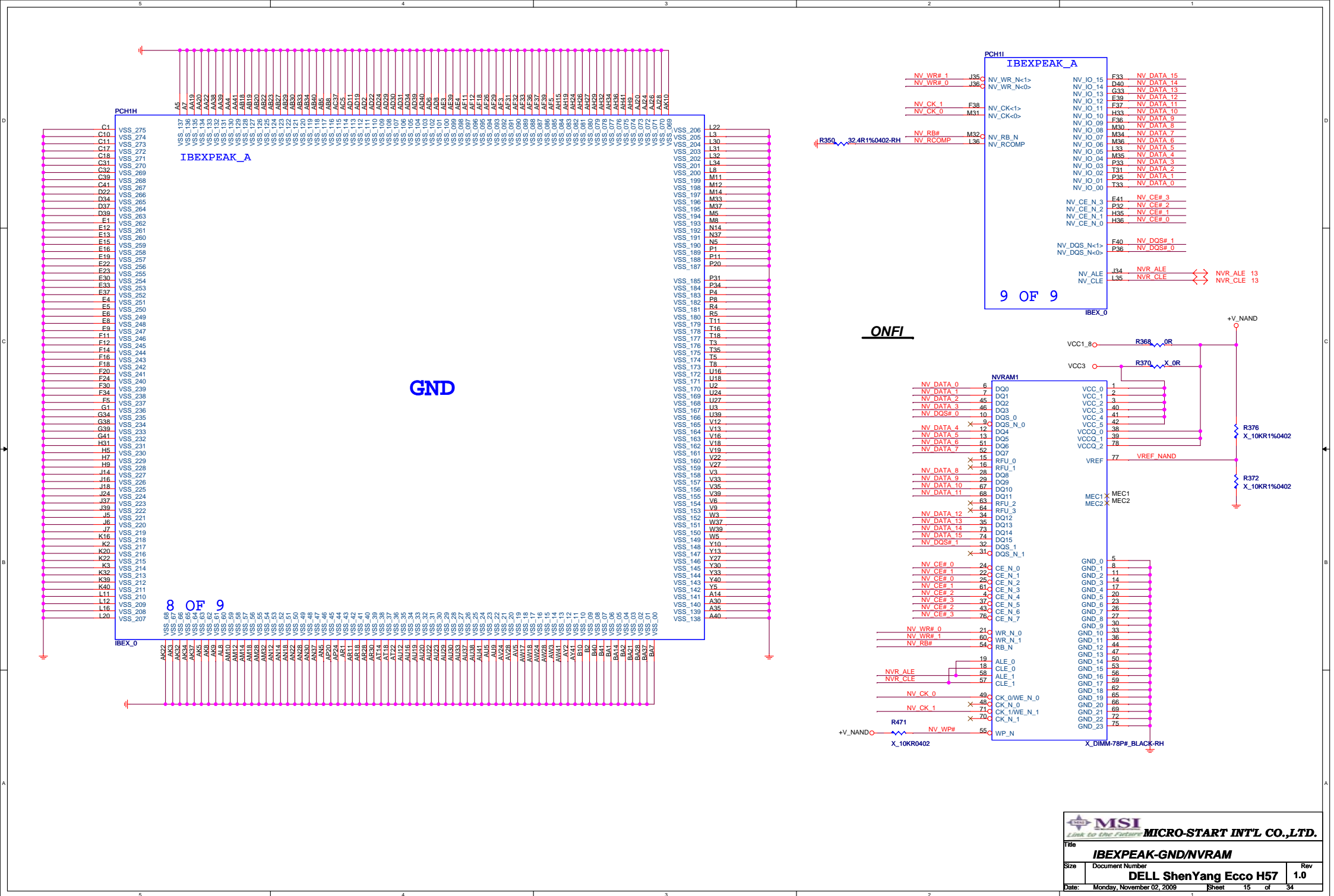


DM1 PLL FILTER

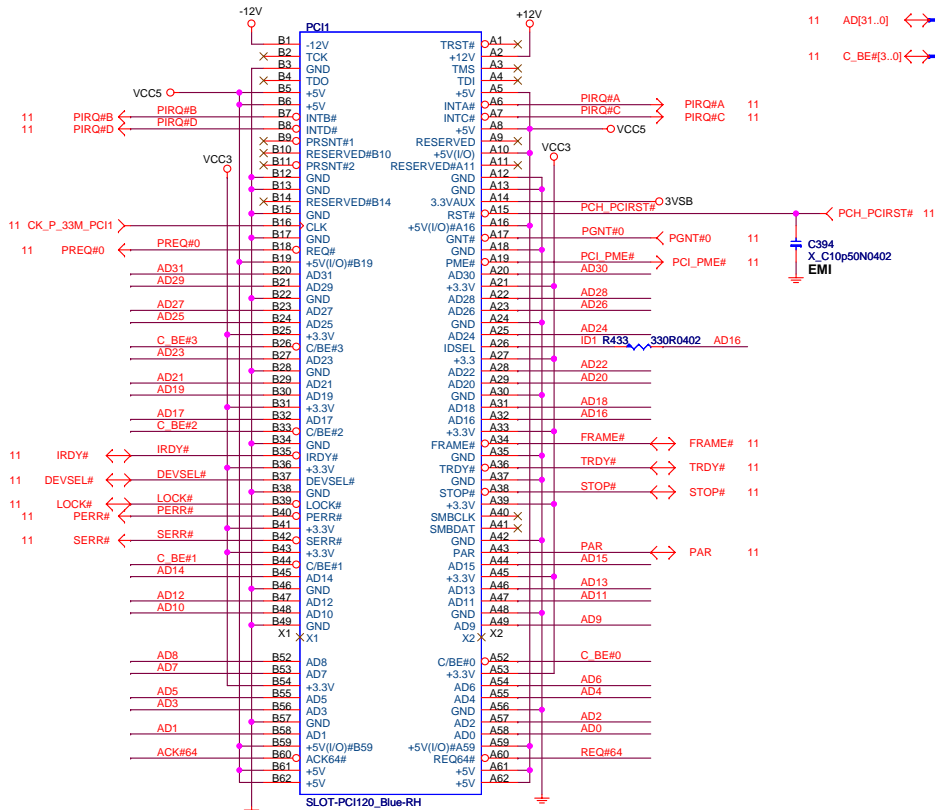


IBEXPEAK_A



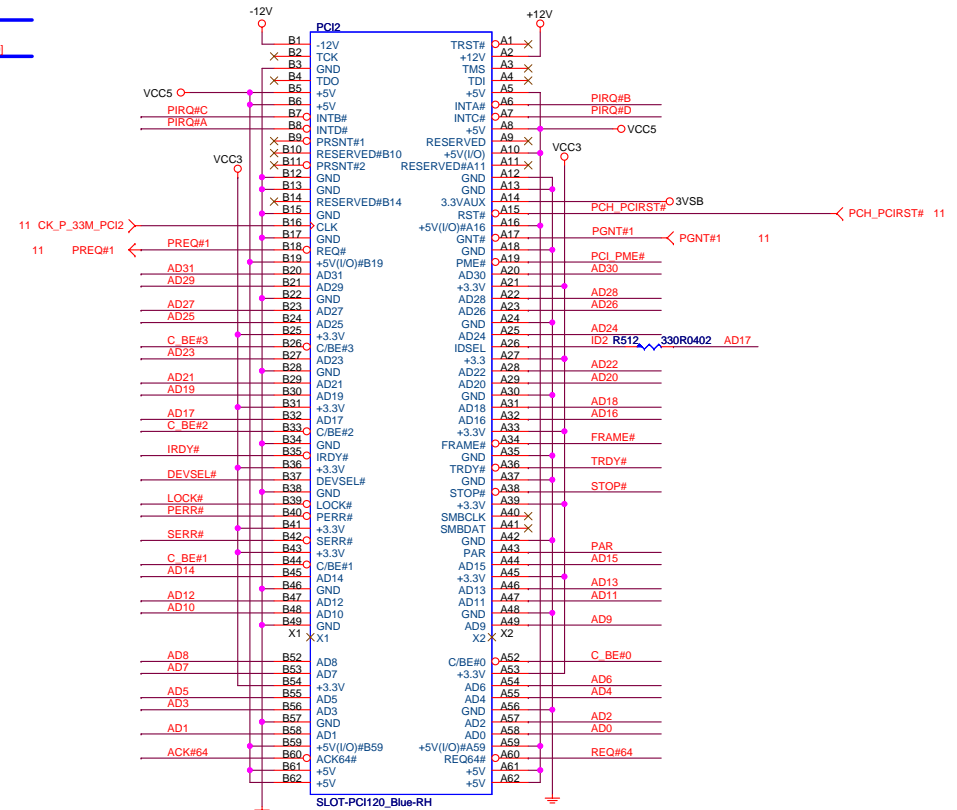


PCI SLOT 1 (PCI VER: 2.2 COMPLY)



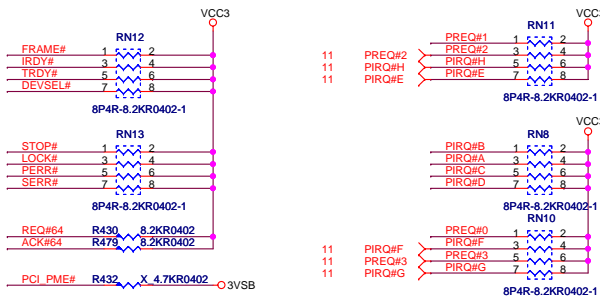
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

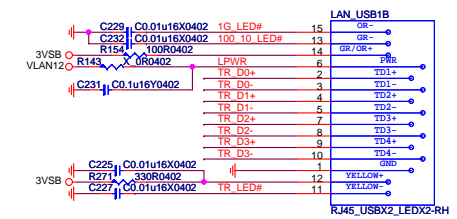
PCI PULL-UP / DOWN RESISTORS



EMI CAPS

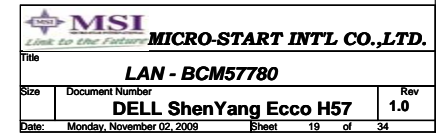


LAN Connector

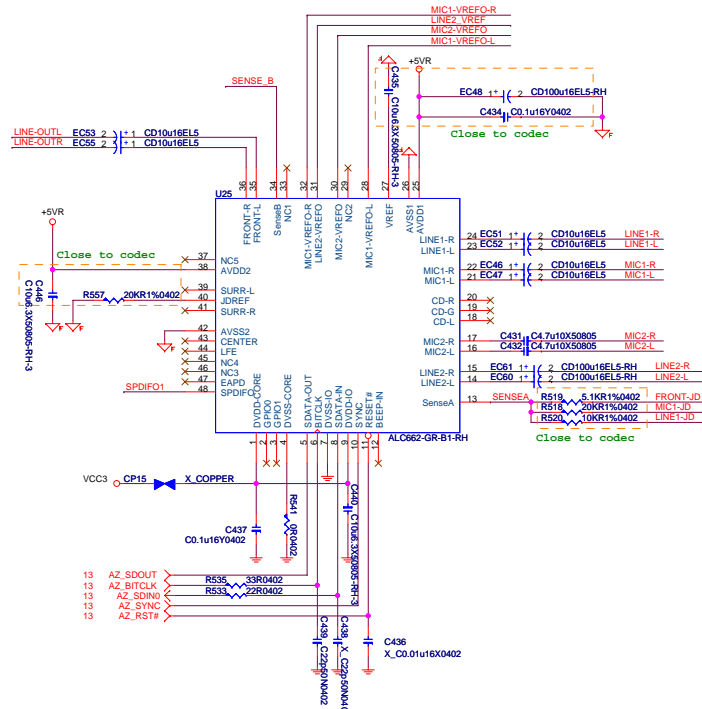


The schematic shows the 24LC02B1T-SN-RH I2C EEPROM connected to the 3V3B supply and GND. The I2C bus is connected to pins 8 (SDA), 7 (SCL), 6 (VCC), and 5 (VSS). The chip is configured with a pull-up resistor (R383) on pin 8 and a pull-up resistor (R402) on pin 7, indicating an I2C address of 0x28. The chip is labeled U23.

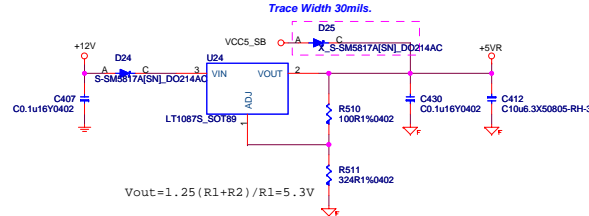
TR D0+	C303	X	C0.1u16Y0402
TR D0-	C302	X	C0.1u16Y0402
TR D1+	C300	X	C0.1u16Y0402
TR D1-	C301	X	C0.1u16Y0402
TR D2+	C299	X	C0.1u16Y0402
TR D2-	C298	X	C0.1u16Y0402
TR D3+	C325	X	C0.1u16Y0402
TR D3-	C322	X	C0.1u16Y0402



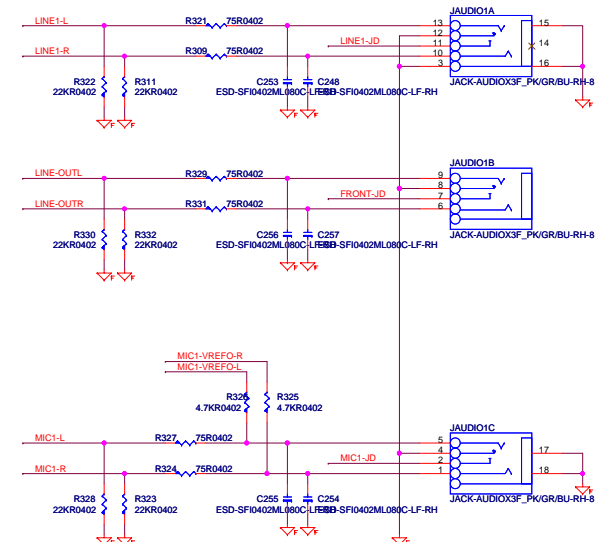
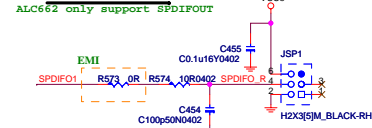
Azalia Codec - ALC662



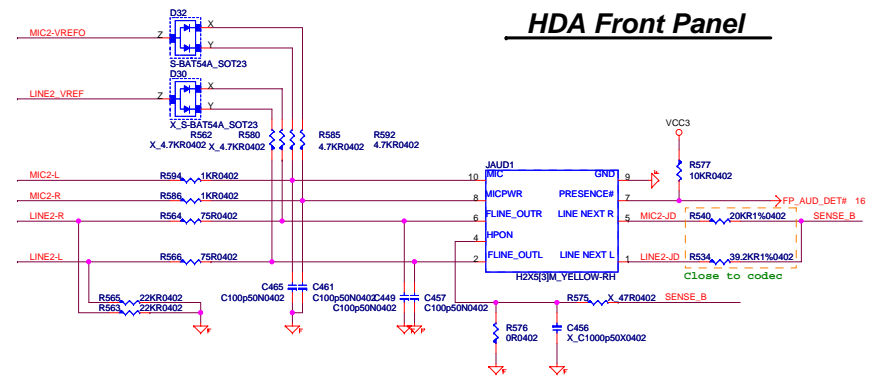
AUDIO CODE REGULATORS



SPDIF OUT

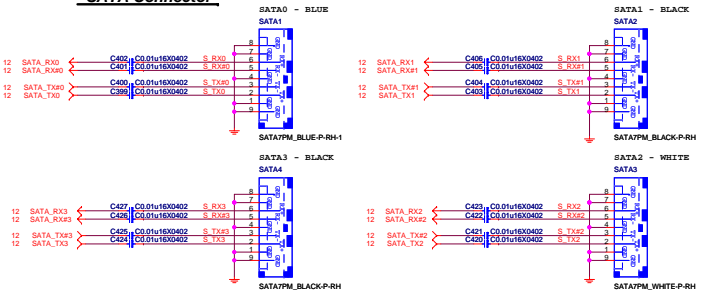


HDA Front Panel

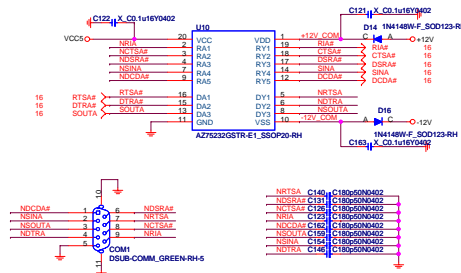


Note the placement need to avoid noise.

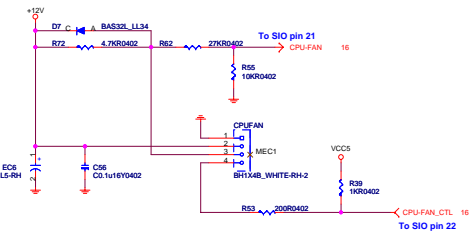
SATA Connector



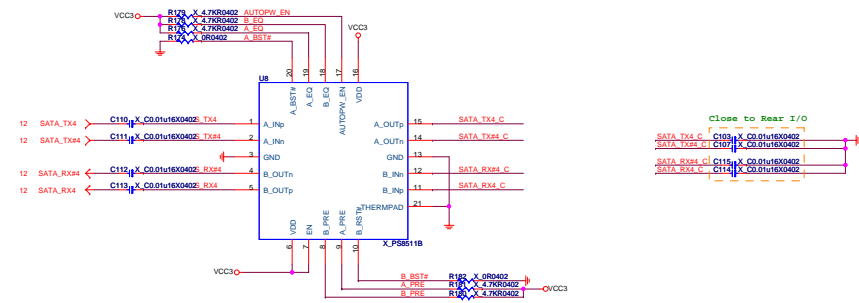
Serial Port



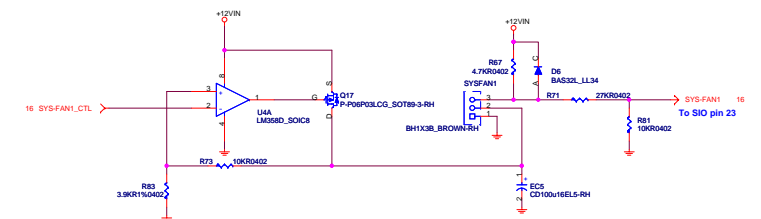
CPU Fan



eSATA Re-Driver (Optional)

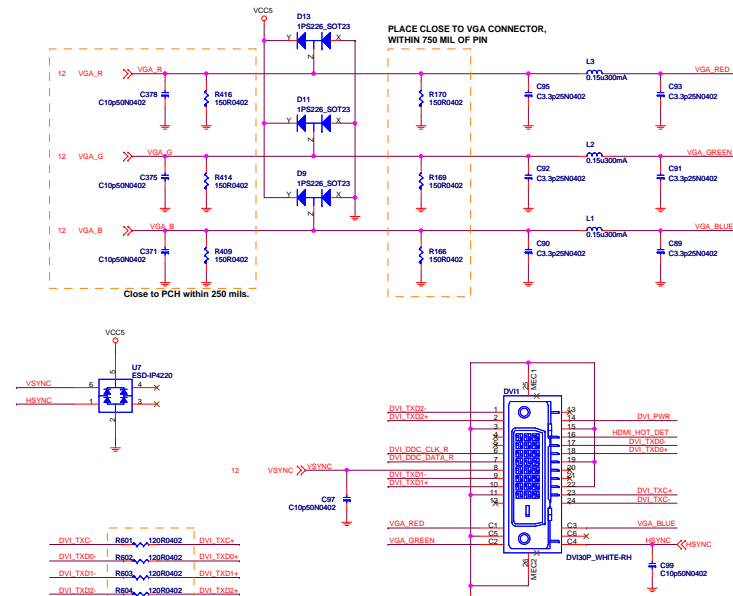
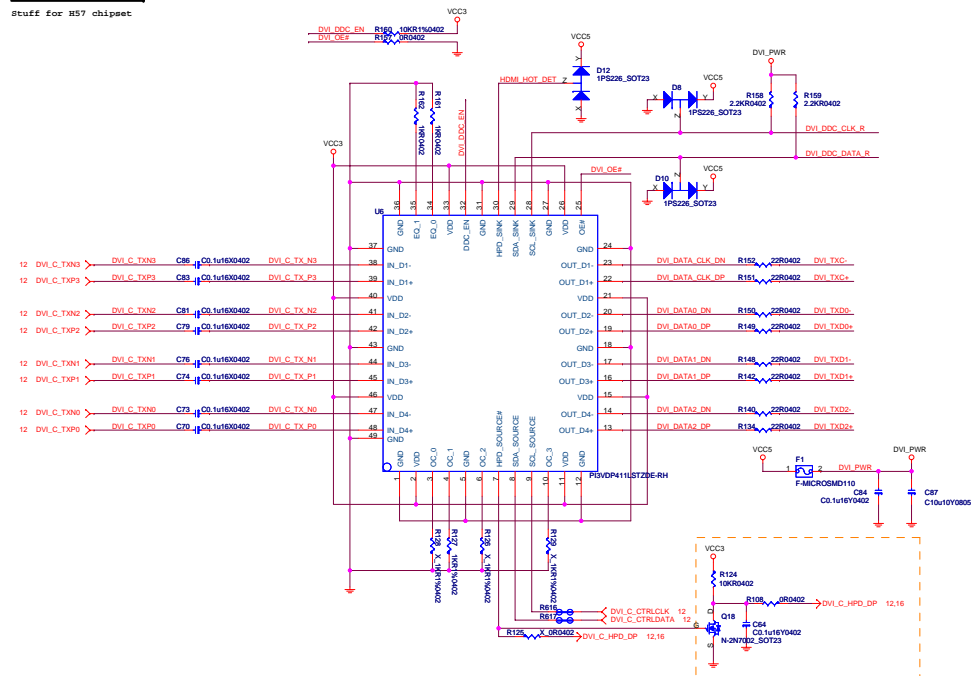


System Fan



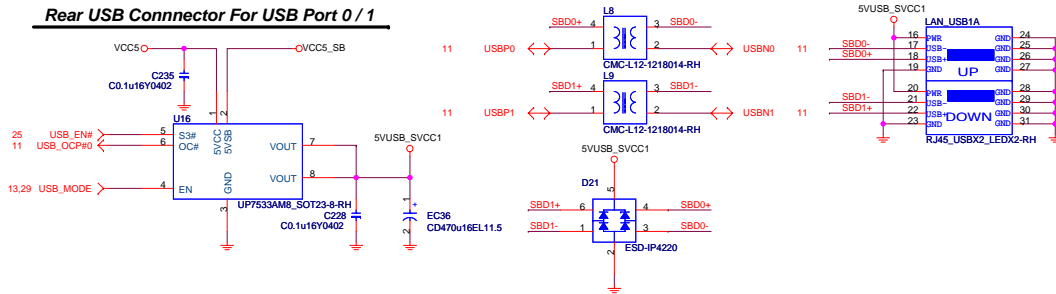
DVI-I Connector

stuff for 357 chipset

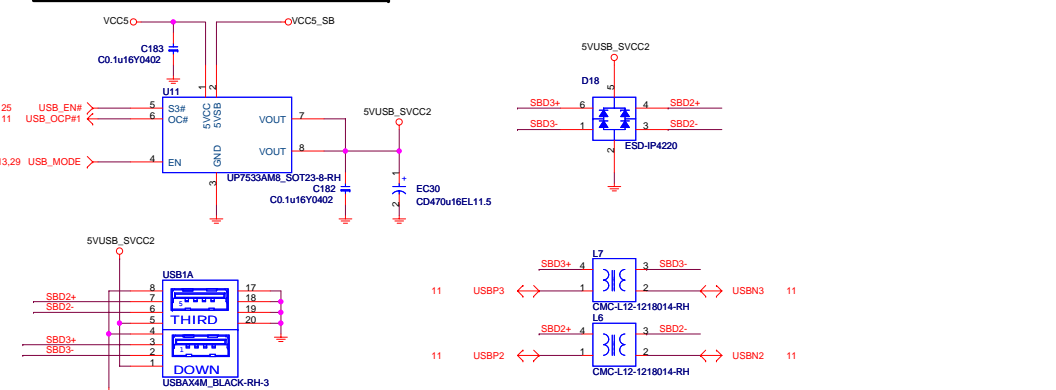


Front Panel and Rear I/O USB Connector

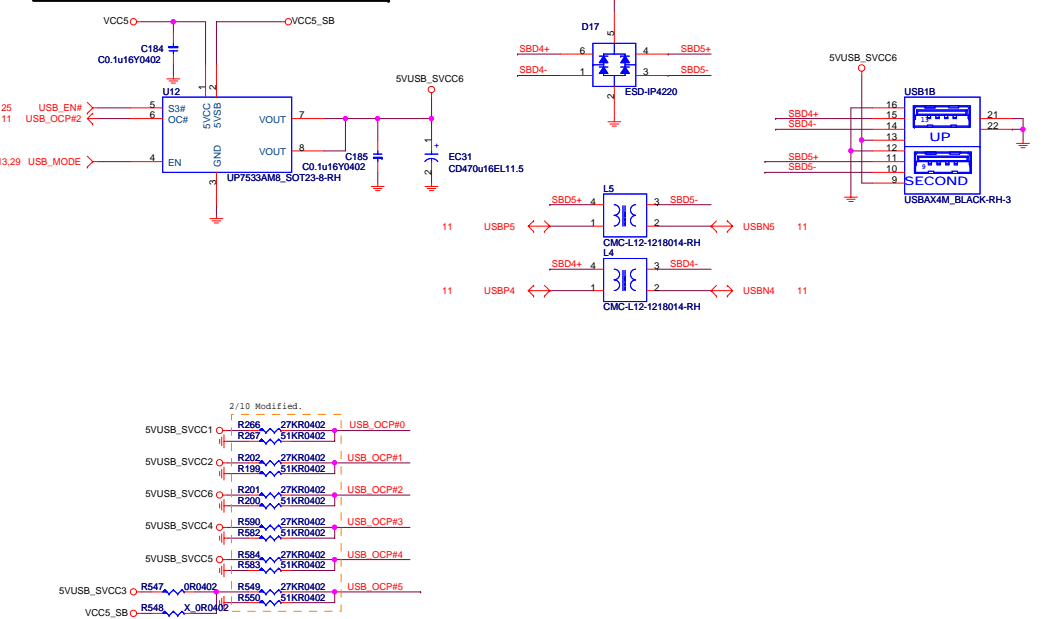
Rear USB Connector For USB Port 0 / 1



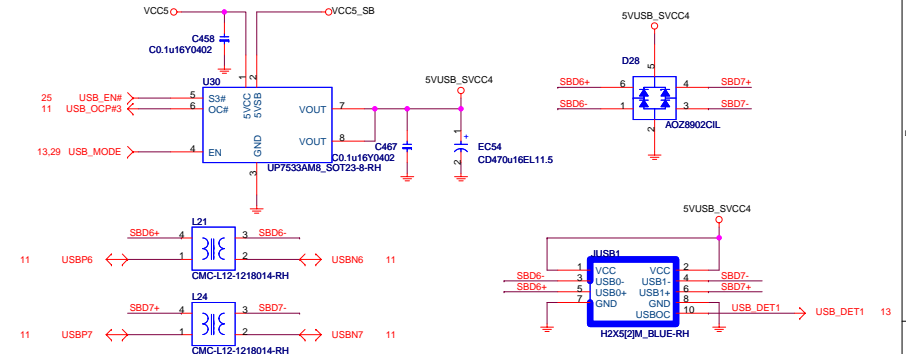
Rear USB Connector For USB Port 2 / 3



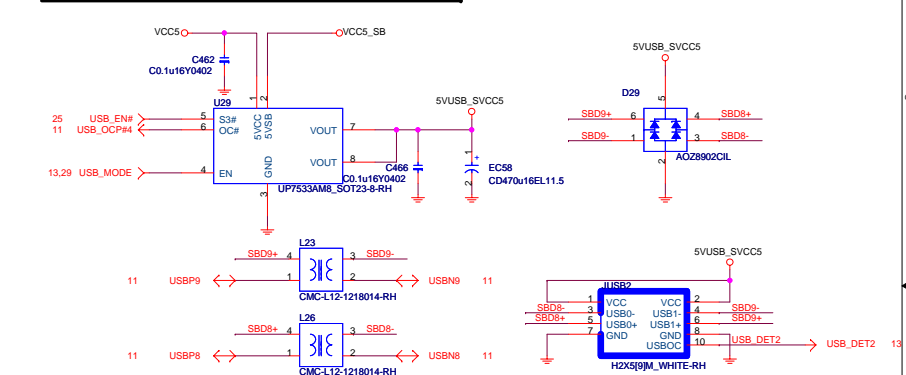
Rear USB Connector For USB Port 4 / 5



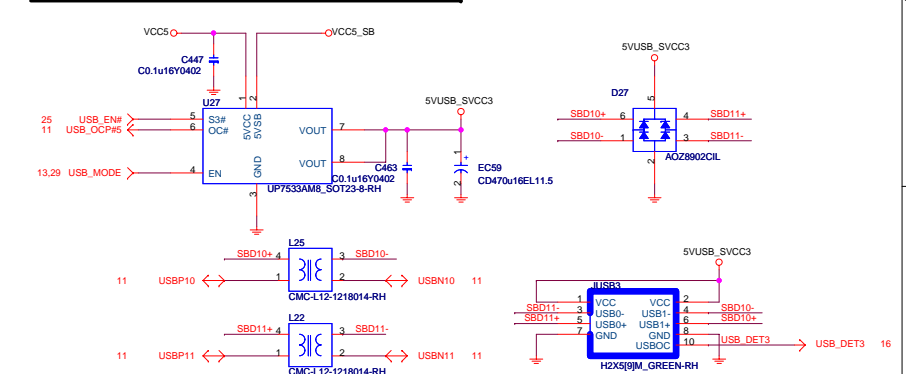
Front Panel USB Connector For USB Port 6 / 7



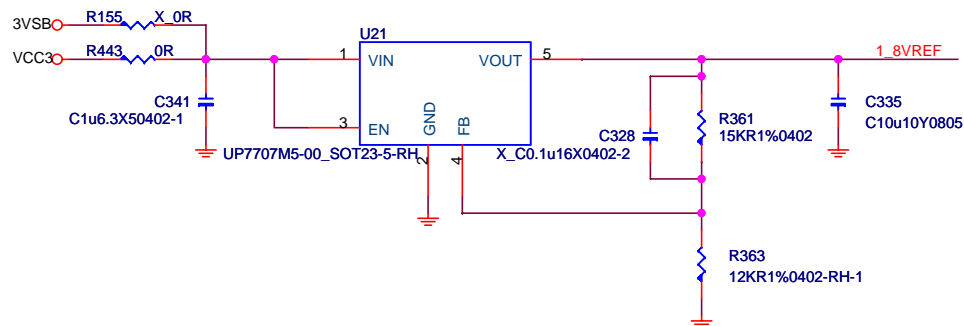
Front Panel USB Connector For USB Port 8 / 9



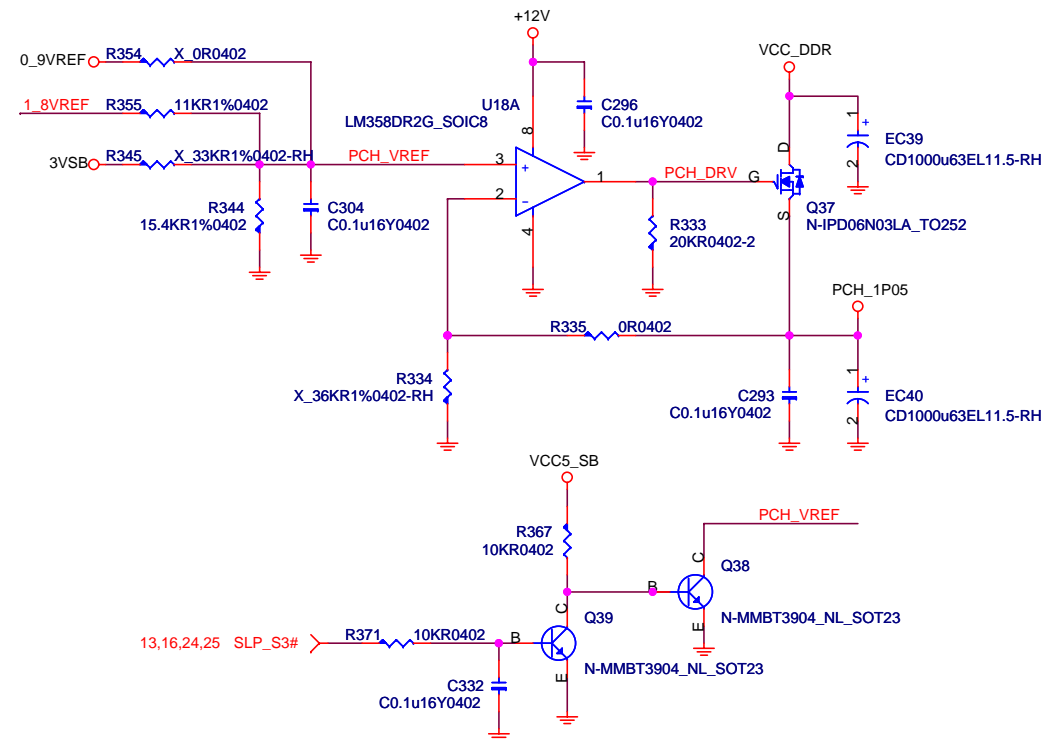
Front Panel USB Connector For USB Port 10 / 11



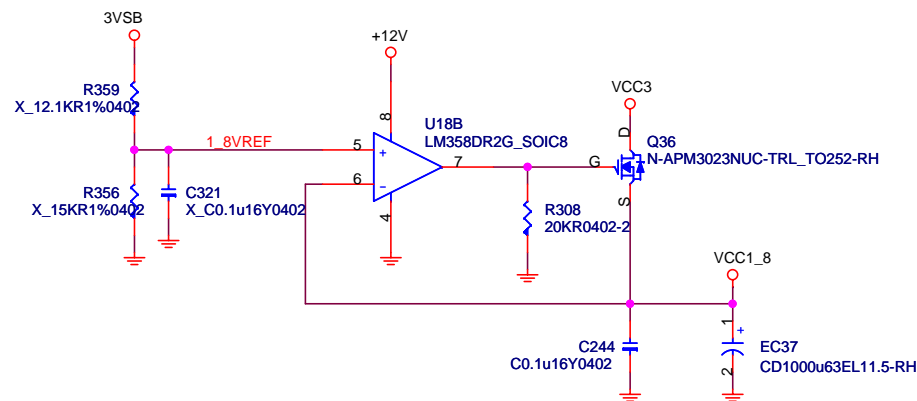
1.8V Reference Power




PCH Core Power 1.05V - 6.5A



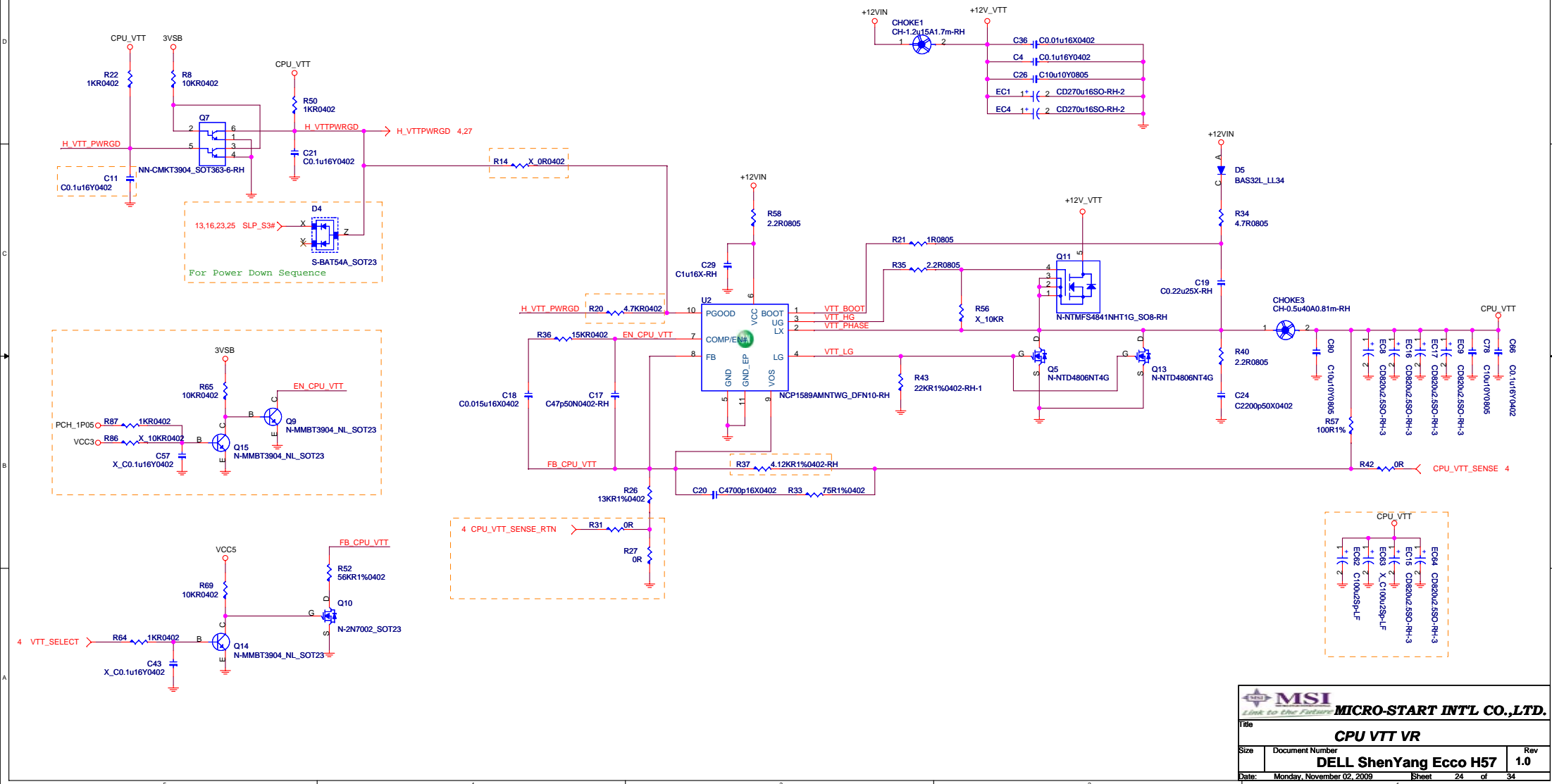
1.8V VSFR 1.5A



 MSI <i>Link to the Future</i>		MICRO-START INT'L CO.,LTD.			
Title					
PCH Core Power					
Size	Document Number				Rev
	DELL ShenYang Ecco H57				1.0
Date:	Monday, November 02, 2009		Sheet	23	of 34

CPU VTT Power

1.1V - 30A - 29W



1.5V - 16A - 29W

DDRIII Regulator Power Source

3.3V - 0.95A - 3.1W

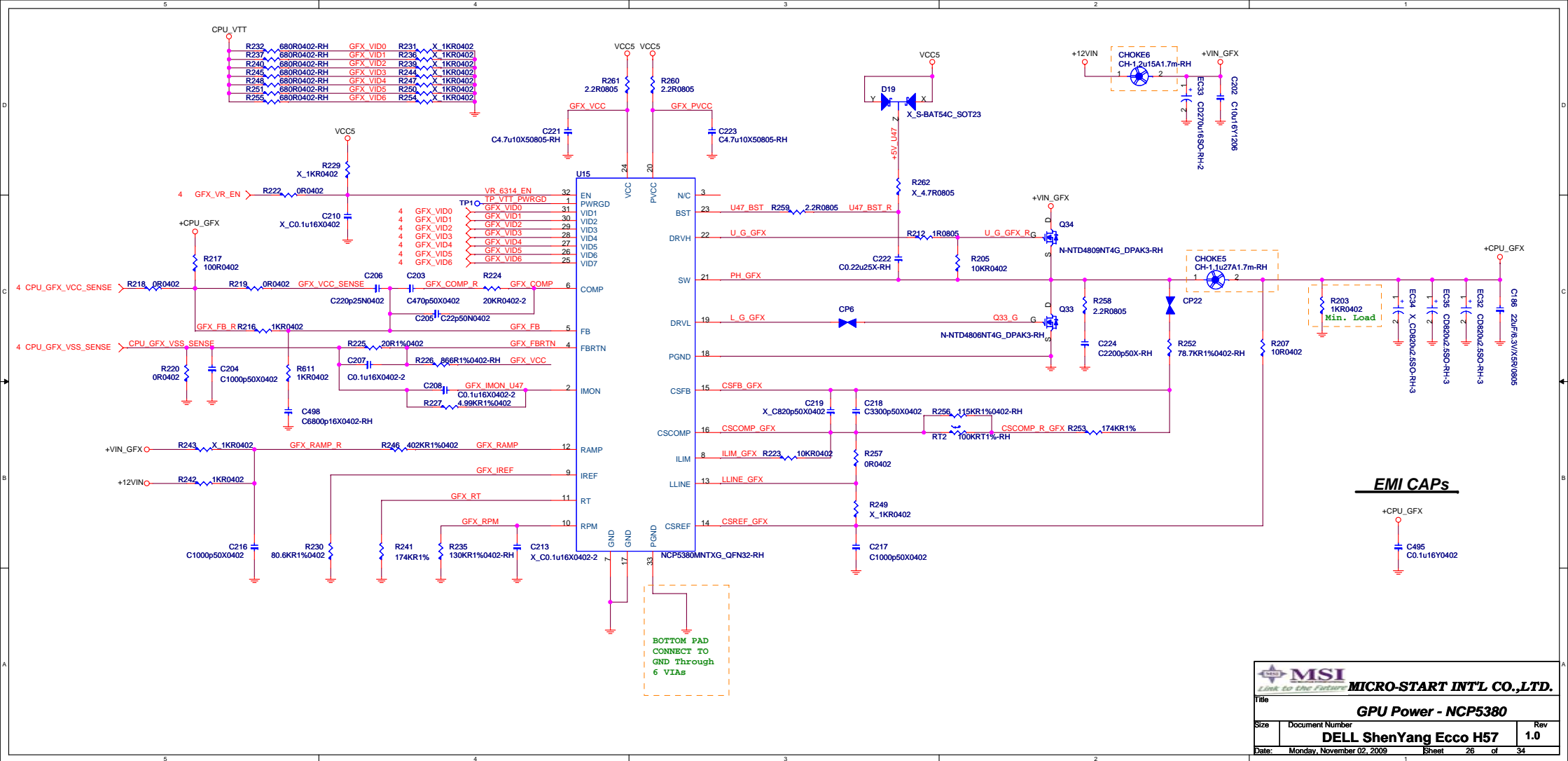
Regulator reference Voltage

DDRIII Termination Power

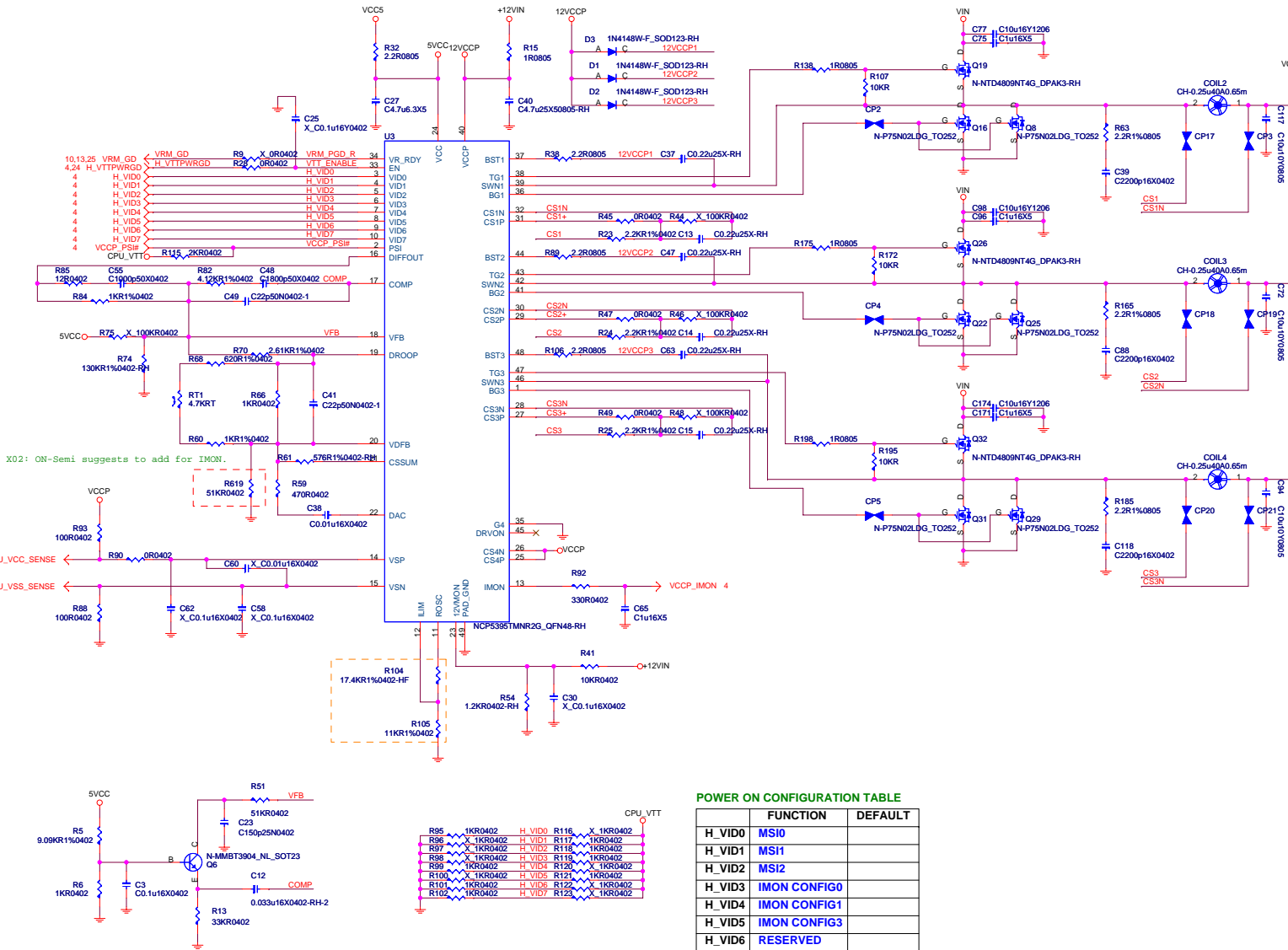
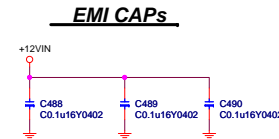
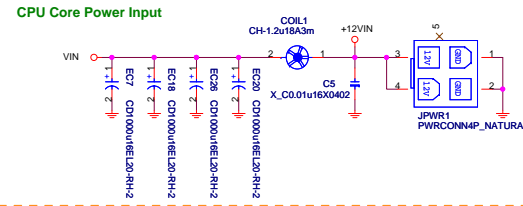
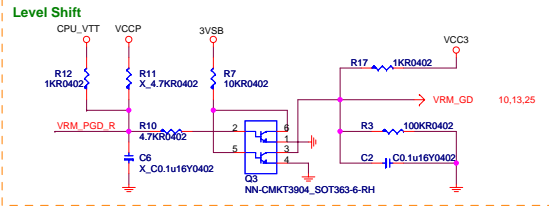
EMI CAPs

DDRIII I/O power decoupling caps.

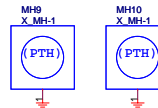
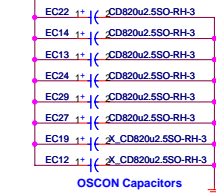
EMI CAPs



Voltage Regular Module (VRD11.1)



Core Power Output cap.

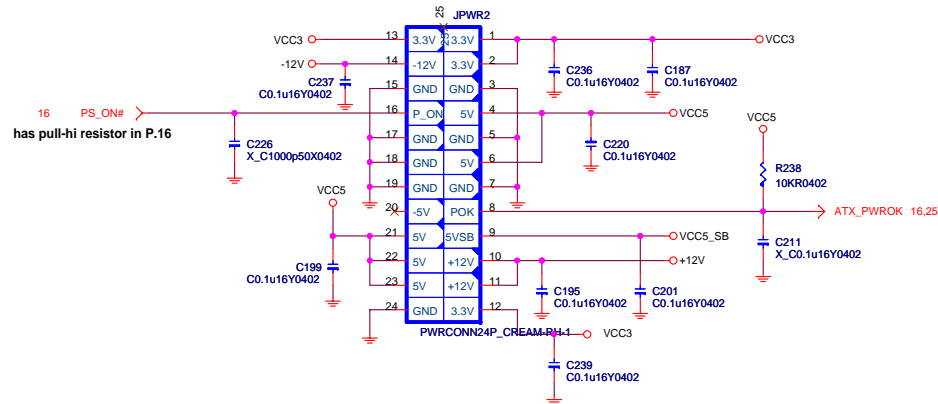


POWER ON CONFIGURATION TABLE

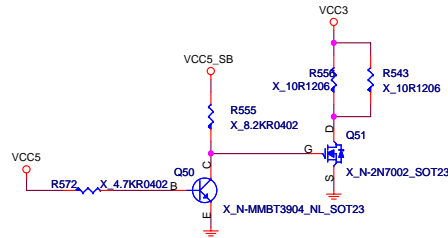
	FUNCTION	DEFAULT
H_VID0	MSI0	
H_VID1	MSI1	
H_VID2	MSI2	
H_VID3	IMON CONFIG0	
H_VID4	IMON CONFIG1	
H_VID5	IMON CONFIG3	
H_VID6	RESERVED	LOW
H_VID7	VRD SELECT	LOW
PSI#	RESERVED	LOW

ATX Power Connector / Front Panel / LED

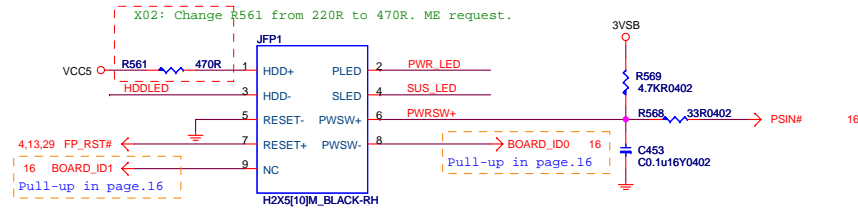
24 Pin ATX Power Connector



Dummy Load

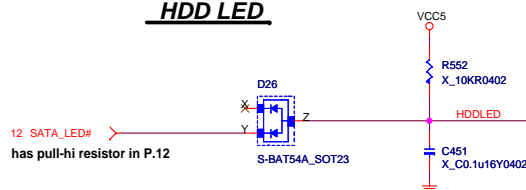


Front Panel



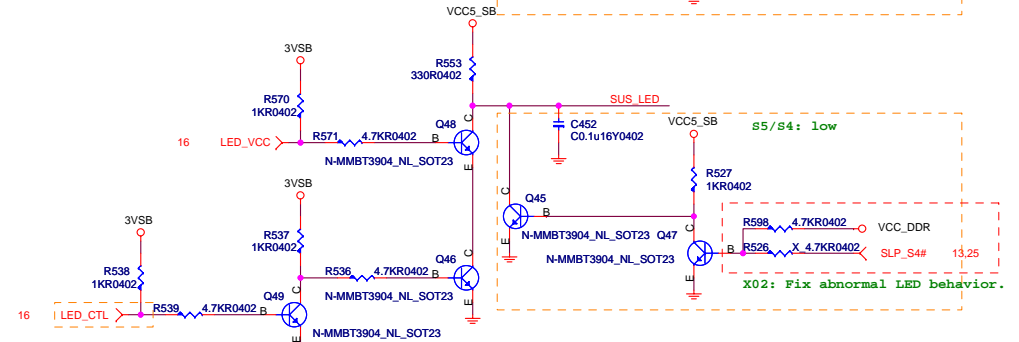
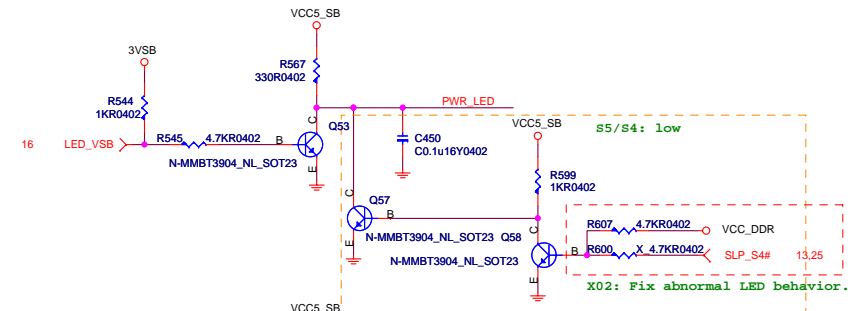
	BOARD_ID0	BOARD_ID1
No Cable	H	H
Shen-Yang	L	L
ECCO	L	H

HDD LED

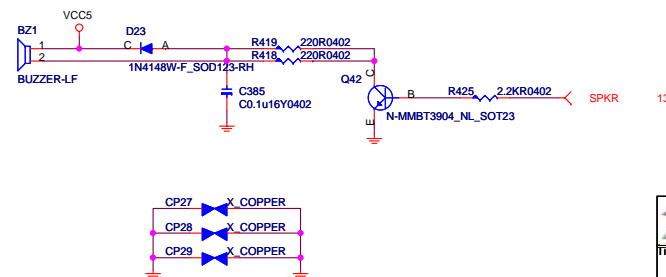


Power LED

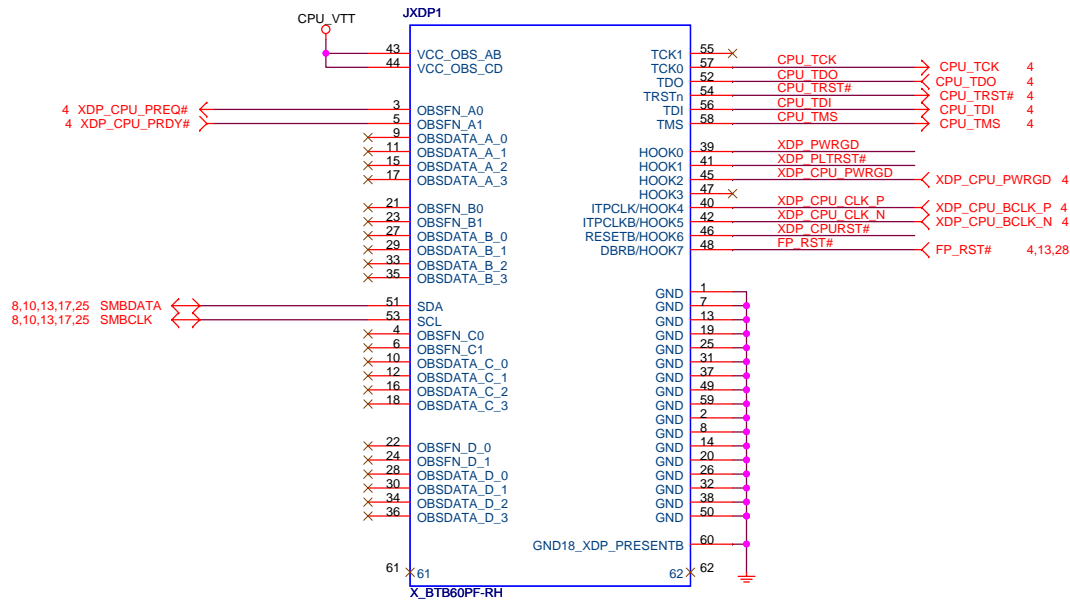
	LED_VSB	LED_VCC	LED_CTL	PWR_LED	SUS_LED
S4/S5	H	H	L	L	L
S0	L	H	L	H	L
S1/S3	Blinking	H	L	Blinking	L
Failure to Post	Blinking	L	L	Blinking	H
No Post	H	H	H	L	H



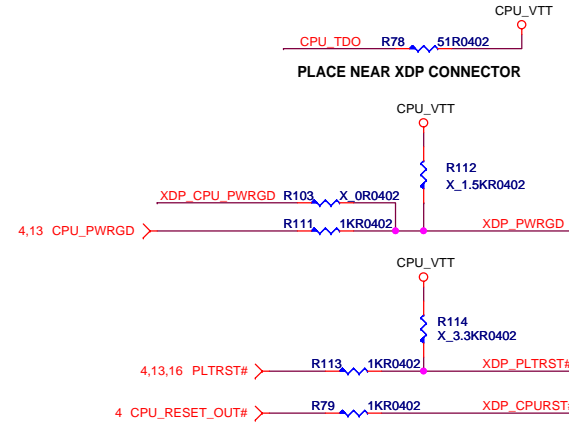
Buzzer Circuit



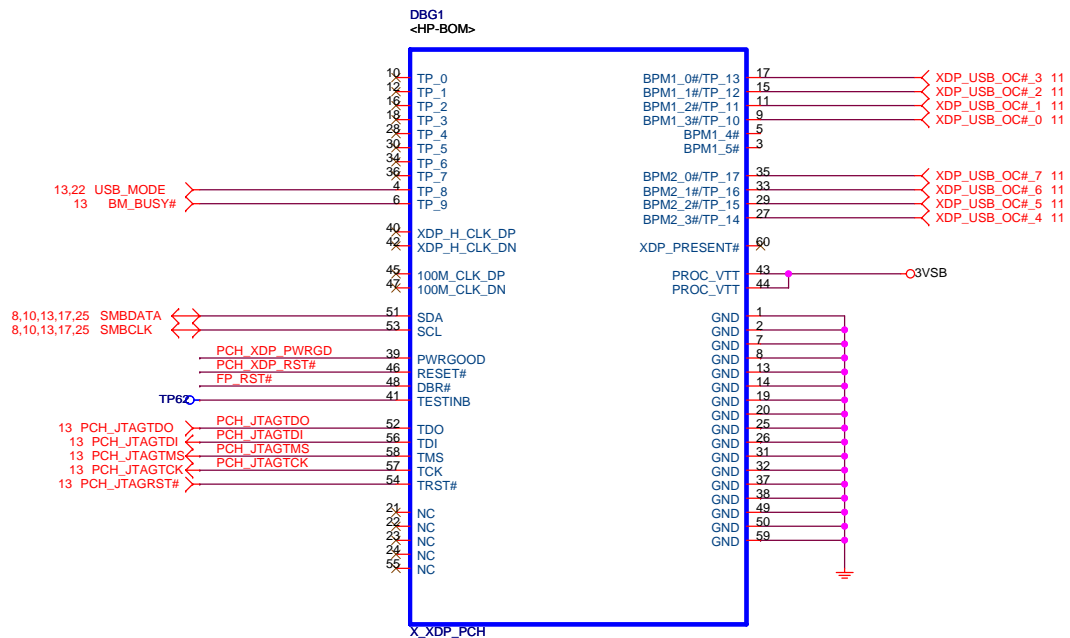
Reserve debug port 5020



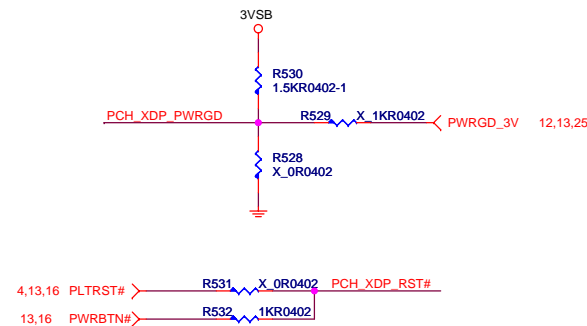
PLACE NEAR XDP CONNECTOR



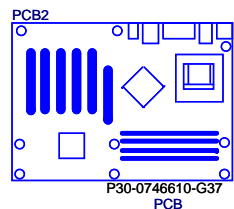
PCH XDP



PCH XDP PWRGD/RESET

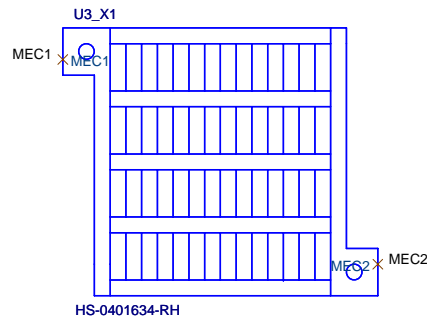
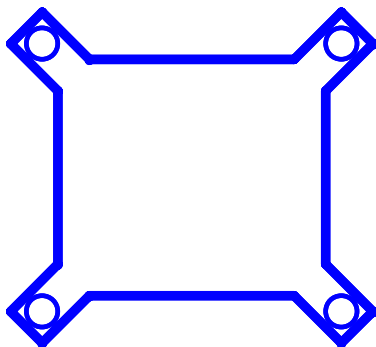


Manual Parts

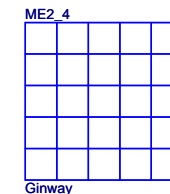
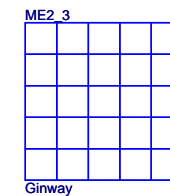
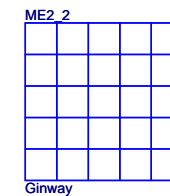
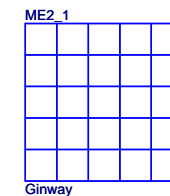
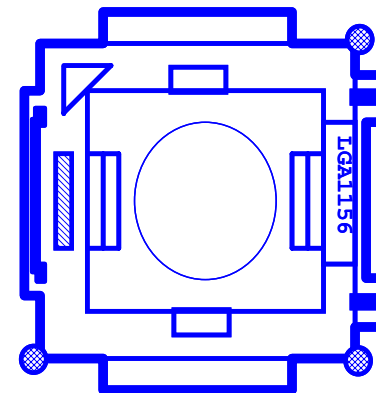


P30-0746610-E55
P30-0746610-G37

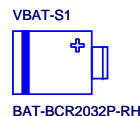
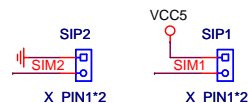
XU1_X2
CPU RETENTION BACKPLATE



XU1_X1
CPU SOCKET

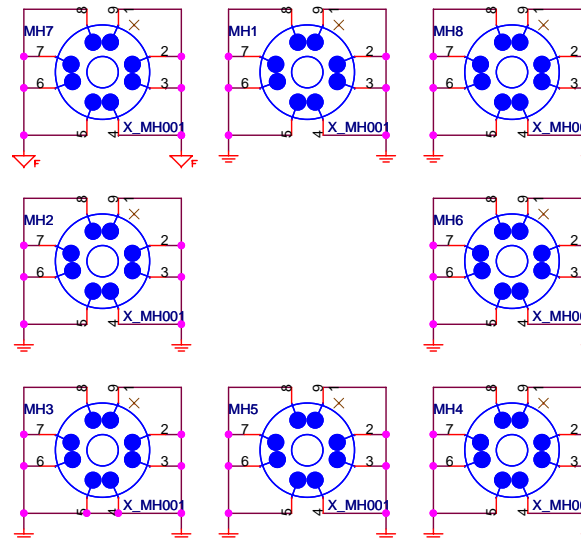


Simulation



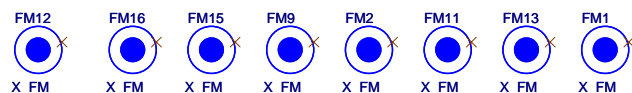
PCB Mounting Holes

Mounting Holes



Optics Orientation Holes

Optical Fiducial Marks-120



Optical Fiducial Marks-100

